KEMING FAN

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INTERESTS

Integrated Circuit Design, Processing in Memory, Hardware Acceleration

EDUCATION

Ph.D., University of California, San Diego, CA, USA — 2022 - Present
Electrical Computer Engineering, Advisor: Tajana Šimunić Rosing, GPA: 3.86/4.0

Bachelor, ShanghaiTech University, Shanghai, China — 2018 - 2022
Electronic Information Engineeringy, GPA: 3.75/4.0

Visiting, University of California, Berkeley, CA, USA — 2021 - 2022
Electrical Engineering & Computer Science, GPA: 3.84/4.0

Graduate Level Courses: Analog Integrated Circuits, VLSI, FPGA, Computer Architecture, Embedded System, Machine Learning, Power Management IC

SKILLS

Language	Chinese (Mandarin), English
Programming Skills	C/C++, Python, Verilog, Tcl, Java
Tools	Cadence Virtuoso, Innovus, Xcelium
	Synopsys VCS, DC
	PyTorch, Vivado, Quartus, Mentor Calibre, ADS

PUBLICATIONS

1. Y. Ding*, **K. Fan***, X. Guo and H. Lyu, "An Ultra-Low-Power Wake-up Receiver with an Integrated PUF ID and Programmable Miss-Detection and False-Alarm Rates," In 2022 7th International Conference on Integrated Circuits and Microsystems (ICICM). IEEE. *(*Equal Contribution)*

RESEARCH EXPERIENCE

RRAM-based Hyperdimensional Computing Accelerator — 10/2022 - Present
SEELab @UCSD, jointly with TSMC — *San Diego, CA*

- Mixed signal tapeout in TSMC40nm in fabrication.
- Designed the analog computing circuits.
- Responsible for RTL verification of digital controller and physical design.

Hyperdimensional Computing Accelerator with Multi-level-cell RRAM — 07/2023 - 11/2023
SEELab @UCSD, jointly with Nanoelectronics Lab @Stanford — *San Diego, CA*

- Post-silicon measurement of a fabricated multi-level-cell (MLC) RRAM chip.
- Proposed a hardware software co-design to achieve faster data processing and energy efficiency improvements for protein analysis.

A Lower Power Wake-up Receiver Design — 11/2020 - 09/2021
Biomedical Integrated Circuit and Microsystem Lab @ShanghaiTech — *Shanghai, China*

- Designed an ultra-low-power wake-up receiver in TSMC180nm for implantable nerve stimulators.
- Derived a math model to calculate the probability of miss detection and false alarm.

COURSE PROJECTS

RISC-V Processor Design in ASAP7nm (Verilog). Implemented RISC-V ISA with 3-stage pipelined CPU. Started from front-end Verilog design, to synthesis, PnR, layout. Verified functionality with gate-level simulation.

Dual-Core 1-D Vector Processor in GPDK45nm (Verilog). Utilized asynchronous FIFOs for clock domain crossing communications. Used pipeline and multi-cycle path techniques to enhance parallelism. Start from RTL design, and ran through the ASIC backend flow using GPDK45nm technology.

AES Secure System Design using Xilinx FPGA (VHDL). Designed an AES encryptor and decryptor supporting 128, 192, and 256-bit key lengths, as well as an automated testbench to ensure functionality.

Operating System Pintos (C). Implemented a simple operating system Pintos, supporting kernel threads, running user programs, as well as a file system under the x86 architecture.

IoT Smart Garden Using Raspberry Pi4 (Python). Implemented a remote plant monitoring and control System, featuring gesture recognition, auto-grow support, and a user-friendly mobile app for real-time status updates.

TEACHING EXPERIENCE

Teaching Assistant at School of EECS, ShanghaiTech University Spring 2019
EE111 Electric Circuits
Instructor: Chaofeng Ye